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REDUCING POWER DISSIPATION IN SELF STARTING AND SELF CORRECTING COUNTER USING A LOOK-AHEAD CLOCK GATING

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ABSTRACT

In this paper, a novel Self-starting and Self-correcting counter implemented with some techniques are presented to reduce the power consumption in sequential circuits. Clock gating is a predominant technique used to reduce unwanted switching of clock signals. Several clock gating techniques to reduce the dynamic power have been developed, of which Data driven method, Auto Gated flip-flop and LACG are predominant. In General way design of Self-starting and Self-correcting counter, it has unfortunately leaves the majority of the clock pulses driving the flip-flops redundant. Data-driven gating aims to disable these and yields higher power saving, but its depends on which FFs should be placed in a group to maximize power reduction. We propose a practical solution based on the toggling activity correlations of FFs and their physical position proximity constraints in the layout and application dependent. The Power consumption of Auto Gated flip-flop is significantly lower than that conventional flip-flops. By using Auto Gated flip-flop, we can replace conventional FFs in Self-starting and Self-correcting counter to achieve reduction of power dissipation. A third method called Look-Ahead Clock Gating (LACG), which combines above two techniques. LACG computes the clock enabling signals of each FF one cycle ahead of time, based on the present cycle data of those FFs on which it depends. It avoids the tight timing constraints of AGFF and data-driven by allotting a full clock cycle for the computation of the enabling signals and their propagation. Simulation results shows that the SSSC counter with the Look-Ahead Clock Gating technique reducing power dissipation on an average of 65.44% compared to the conventional SSSC counter and data-driven clock gating SSSC counter.

KEYWORDS: Self-starting and Self-correcting (SSSC) counter, Auto Gated flip-flop (AGFF), Look-Ahead Clock Gating (LACG).

INTRODUCTION

Now a days, general-purpose digital circuit designs are faced with the daunting task of reducing power dissipation since power dissipation is quickly becoming a bottleneck for future technologies. Lowering power consumption is important for not only lengthening battery life in portable systems, but also improving reliability, and reducing heat-removal cost in high-performance systems.

Clock power is a major component of consumer electronic products. Power mainly because the clock is fed to most of the circuit blocks in the processor, and the clock switches every cycle. The system's clock signal, typically responsible for 30% to 70% of the total dynamic (switching) power consumption [1].

Clock gating is a well-known technique to reduce clock power. Because individual circuit usage varies within and across applications, not all the circuits are used all the time, giving rise to power reduction opportunity. By ANDing the clock with a gate-control signal, clock gating essentially disables the clock to a circuit whenever the circuit is not used, avoiding power dissipation due to unnecessary charging and discharging of the unused circuits. Specifically, clock gating targets the clock power consumed in pipeline latches and dynamic-CMOS-logic circuits (e.g., integer units, floating-point units, and word line decoders of caches) used for speed and area advantages over static logic.

Effective clock gating, however, requires a methodology that determines which circuits are gated, when, and for how long. Clock-gating schemes that either result in frequent toggling of the clock-gated circuit between enabled and disabled states, or apply clock gating to such small blocks that the clock-gating control circuitry is almost as large as the blocks themselves, incur large overhead. This overhead may result in power dissipation to be higher than that without clock gating. While the concept of circuit-level clock gating is widely known, good architectural

methodologies for effective clock gating are not. Data driven method, Auto Gated flip-flop and LACG are recent techniques [2], which essentially outlines a predictive clock-gating methodology

To explain the Data driven method, Auto Gated flip-flop and LACG techniques it is applied in a simple Self-Starting and Self-Correcting Counter circuit.

In normal Self-starting and Self-correcting (SSSC) counter consumes large dynamic power dissipation. A Self-starting and Self-correcting (SSSC) counter is constructed based on application requirement by N number of flip flops. This novel paper presents the three methods to reduce power dissipation and increases the speed of the operation in Self-starting and Self-correcting (SSSC) counter.

Circuit-level clock gating focuses on clock-gating finite state machines (FSM) [3]. The limitation of gated-clock FSM is that its power saving heavily depends on the FSM characteristics.

The rest of the paper is organized as follows. Section II discusses related Self-starting and Self-correcting counter design. Section III describes Data-driven clock gating method, by using this method to implemented SSSC counter .Section IV low power flip-flop design that is Auto Gated Flip-Flop and SSSC counter design by using AGFF. In Section V, details of a new method called look-Ahead clock gating technique Section VI presents the results and Section VII concludes the paper.

SELF-STARTING AND SELF-CORRECTING (SSSC) COUNTER

The counter always starts counting sequence from either 000 or 111.but, real time environment, the counter will not always start from this predefined count value. As soon as the power switch is ON, the states of the flip-flops is undefined, they will be set or reset at random. Therefore, the counter should not be able to start from any predefined state and the counting states will not be correct. This problem can be eliminated by self-starting and self-correcting counters.

In any mod-n counter, all possible states are not present but only required states are present. But a self-starting counter each possible states which are not desired count sequence. The Self-starting and Self-correcting counters should have a sequence of transition that leads to valid counter states.it is not a matter how the counter starts up, but it eventually enters the proper counter sequence after very short time.

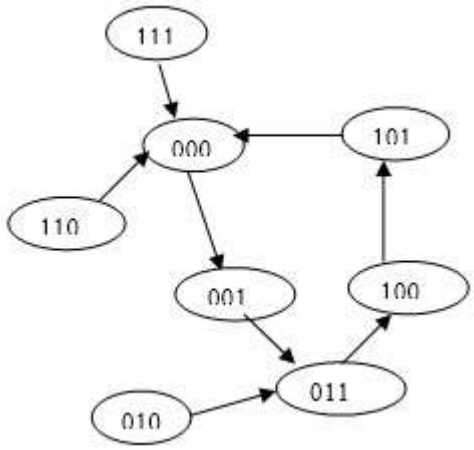

Fig: 1. State transition diagram of a Self-starting and Self-correcting counter.

Figure 1 shows the state transition diagram of a typical self-counting counter. In this state transition diagram, the counter should be in sequence after one transition. In this diagram, counter may require one transition before entering into the correct sequence. During design, it is necessary to select the counter sequence as few transitions as possible. Therefore, fig1 is used for hardware implementation.

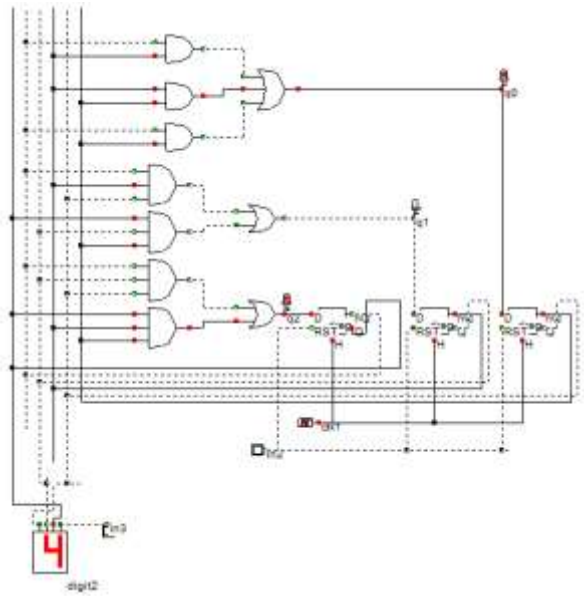

Fig: 2. Self-starting and Self-correcting counter

As shown in fig 2 the counting sequence is 000,001,011,100,101,000.if at starting initial count value is either 111 or 110 or 010, then self-correcting capability has been added after incorporating the unused states in counter design. If present state is 111 or 110 then, next transition will be 000. When present state is 010 then next state transition is 011. When this counter is designed with D flip-flops, the excitation of d flip-flops, the excitation of D flip flops will be the next state. Flip-flops excitation for self-starting counter is used to implement logic circuits to generate input to the sequential element (FFs). The state transitions are used to represent by k-maps to minimize logic circuit.

In some applications of counters, self-initialization is an advantage. It eliminates the need for complex initialization and guarantees the return to the original state sequence after a temporary wrong state. The low operating frequency and large areas of available self-correcting counters have limitations. Due to the additional hardware required to change state transitions, the final circuit tends to be slow and large. The self-starting and self-correcting counters have maximum 10 stages.

In the preceding discussion, our primary goal was to enter the count sequence at a valid state. The particular starting state did not matter. Although this may be true in some applications, it is more usual to have a distinguished starting state for the counter or finite state machine. If this is the case, it is desirable to include additional hardware to reset the counter to this state. We can accomplish this with an explicit reset button or a special resistor/capacitor circuit that asserts the reset signal for a short time after power up. Flip-flops typically come with preset and clear inputs. Thus, we can use an asserted reset signal to place the flip-flops in the desired starting state. The implementation in Figure2 includes such circuitry to reset the flip-flops to state 000. Of course, by judicious use of preset inputs as well as clear, we can choose any state as the starting state.

DATA -DRIVEN CLOCK GATING METHOD

Clock enabling signals are very well understood at the system level and thus can effectively be defined and capture the periods where functional blocks and modules do not need to be clocked. Those are later being automatically synthesized into clock enabling signals at the gate level. In many cases, clock enabling signals are manually added for every FF as a part of a design methodology. Still, when modules at a high and gate level are clocked, the state transitions of their underlying FFs depend on the data being processed. It is important to note that the entire dynamic power consumed by a system stems from the periods where modules' clock signals are enabled. Therefore, regardless of how relatively small this period is, assessing the effectiveness of clock gating requires extensive simulations and statistical analysis of FFs toggling activity, as presented subsequently.

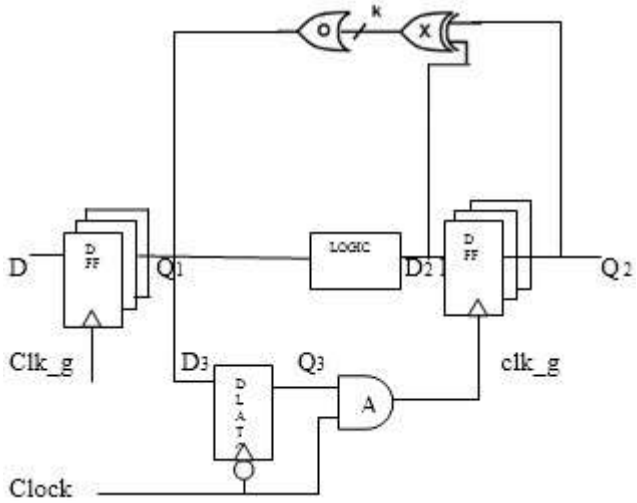

Fig. 3. Circuit implementation of data-driven clock gating.

Shown in figure. 3 Data driven clock gating design. Here FFs founds out that its clock can be enable or disabled in the next cycle [5]. Input D2 of a particular FF and output Q2of same FF is comparison by on XOR gate. The output of K XOR gates are connected to OR gate to generate a joint clock gating signal for K flip-flops [6]. Which is then latched to avoid glitches. The combination of a latch with AND gate is used by commercial tools and is called Integrated Clock Gate (ICG). Data-driven gating suffers from a very short time-window where the gating circuitry can properly work. The cumulative delay of the XOR, OR, latch and the AND gater must not exceed the setup time of the FF. Another difficulty of data-driven gating is its design methodology, to reduce the hardware overhead involved and to maximize power savings, the flip flops should be grouped.so that they share a common clock enabling signal. The question of what is the group size maximizing the power savings is depends upon application switching activities.

In General way design of Self-starting and Self-correcting counter, it has unfortunately leaves the majority of the clock pulses driving the flip-flops redundant. Data-driven gating aims to disable these and yields higher power saving than that of without clock gating. Self-starting and Self-correcting counter implementation with data-driven clock gating technique show in figure 4.

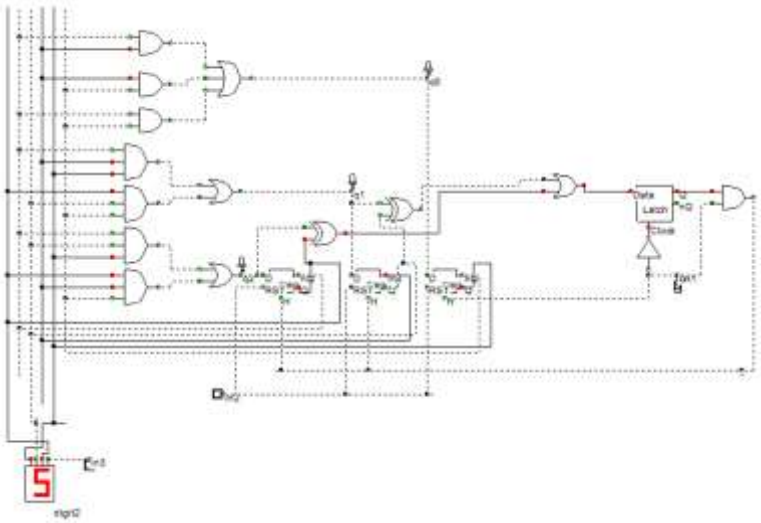

Fig. 4. Self-starting and Self-correcting counter implementation with Data-driven clock gating technique.

How flip-flops grouped? Which FFs should be placed in a group to maximize the power reduction [7]? We propose a practical solution based on the toggling activity correlations of FFs and their physical position proximity constraints in the layout.

In Self-starting and Self-correcting counter counting sequence is 000,001,011,100,101,000. Here observe that DFF2 and DFF1 flip-flops are grouped based on the toggling activity correlation of FFs. This requires running extensive simulations characterizing the typical applications expected by the end-user. Those applications are in many cases unknown and the amount of redundant clock pulses may significantly increase for specific applications.

AUTO GATED FLIP- FLOP

A new flip-flop is presented in which power dissipation is reduced by deactivating the clock signal on slave latches when there are no data transitions [8]. The power consumption of the presented circuit is significantly lower than that of a conventional flip-flop when the D input has a reduced switching activity.

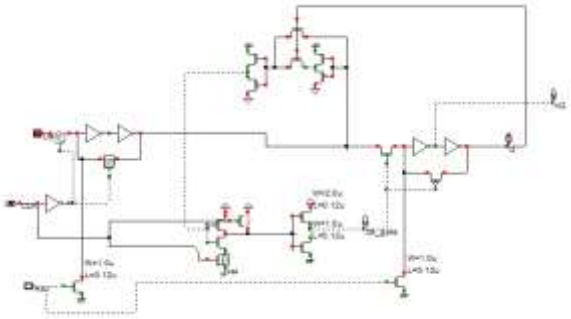

Fig.5. Schematic diagram of Auto Gated Flip-Flop.

A simplified schematic diagram of Auto Gated Flip-Flop is shown in Fig.5. Here shows that dotted lines and thick lines, which are represented logic '0' and logic '1' respectively. The slave latch is positive level-sensitive (it is transparent when clkg = 1 and on hold for clkg = 0). The comparison between D and Q is performed by an XOR gate, while the gating Logic circuit compromises a simple AND gate. The operation of the circuit is as follows. If clk is 0, then clkg is also 0 and the slave latch is correctly in the hold state. On the other hand, when clk is high and D is different from Q, the gating logic enables the clkg signal so that the latch can correctly switch. Note that if D is equal to Q the gating logic inhibits the propagation of switching activity from clk to clkg. In this way the power consumption is reduced, assuming that the capacitance on the clkg node is higher than the input capacitance of the gating logic.

The basic circuit used for LACG is Auto-Gated Flip-Flop (AGFF) illustrated in Fig. master latch becomes operated on the falling edge of clock. Slave latch becomes operated on the raising edge of clock gating signal. The XOR gate indicates whether or not the slave latch should change its state. If it does not, its clock pulse is stopped and otherwise it is passed. If it does not, its clock pulse is stopped and otherwise it is passed. In a significant power reduction was reported for register-based small circuits, such as counters like self-starting and self-correcting counters, where the input of each FF depends on the output of its predecessor in the register.

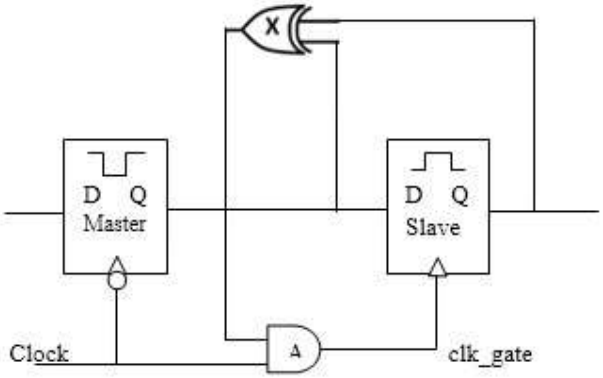

Fig.6.a). an Auto Gated Flip-Flop.

Auto-Gated Flip-Flip (AGFF) method is very simple to implemented shown in figure 6.a) and can be used for general logic by allotting a full clock cycle for the computation of the enabling signals and their propagation. So we can able to use in self-starting and self-correcting counters. But it has two main drawbacks. 1). only the slave latches are gated, leaving half of the clock load not gated.2). Serious timing constraints are imposed on those FFs residing on critical paths, which avoid their gating.

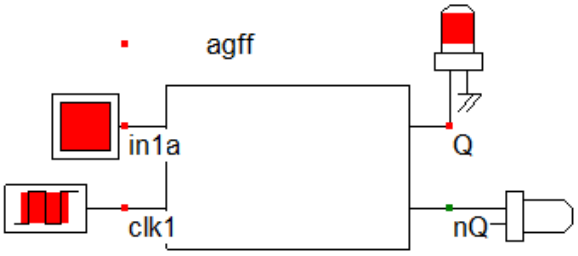

Fig.6.b). An Auto Gated Flip-Flop symbol

Self-starting and Self-correcting counter implemented with Auto-Gated Flip-Flips are presented to reduce the power consumption in sequential elements. Shown in figure.6.b) Auto-Gated Flip-Flip symbol. Table1 shows power dissipation of the AGFF is significantly lower than that of a conventional flip-flop when the D input has a reduced switching activity.

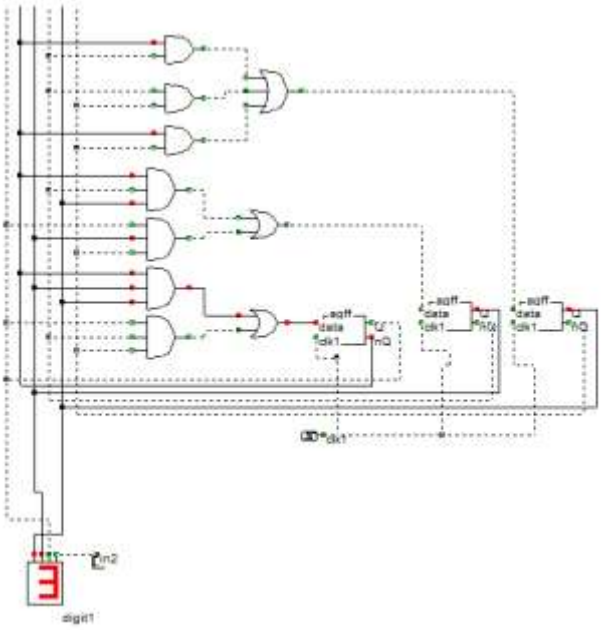

Fig.7. Self-Starting and Self-Correcting Counter with Auto Gated Flip-Flops.

Self-Starting and Self-Correcting Counter with Auto Gated Flip-Flops is illustrated in fig.7. The power consumption increased due to the power dissipation in the circuits. Most of the power dissipation occurs due dynamic power. In normal Self-Starting and Self-Correcting Counter consumes large dynamic power dissipation. To reduce the power dissipation in sequential circuit by using Auto Gated Flip-Flops.

LOOK-AHEAD CLOCK GATING (LACG)

To overcome the above problems, a novel technique called look-Ahead clock gating is used which combines above all the two methods. Look-ahead clock gating has been shown to be very useful in reducing the clock switching power. The computation of the clock enabling signals one cycle ahead of time avoids the tight timing constraints existing in

other gating methods. A closed form model characterizing the power saving was presented and used in the implementation of the gating logic. The gating logic can be further optimized by matching target FFs for joint gating which may significantly reduce the hardware overheads. This simplification is advantageous as it significantly simplifies the gating implementation.

Auto-Gated Flip-Flops are grouping in look-Ahead clock gating, addressing three goals 1). Stopping the clock pulse also in the master latch. 2).This technique applied in large and general designs and eliminate the tight timing constraints.

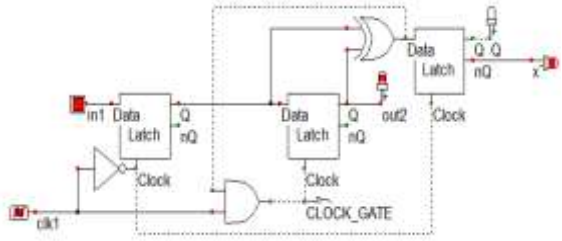

Fig .8.a). Enhanced AGFF with XOR output used for LACG.

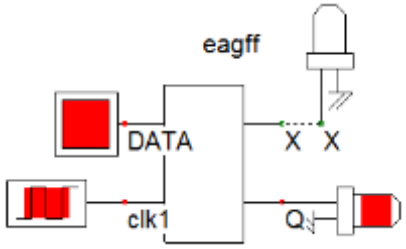

Fig .8.b).Symbol of the enhanced AGFF with the XOR output.

LACG is based on using the XOR output in Auto Gated Flip-Flops. To generate clock enabling signals of other FFs in the system, whose data depend on that FFs. There is a problem though. The XOR output is valid only during a narrow window [FF's setup time and clock to output contamination delay] of around the clock rising edge. After a delay the XOR output is corrupted and turns eventually to zero. To be valid during the entire positive half cycle it must be latched as shown in Fig. (a). Fig. (b) Is the symbol of the enhanced AGFF with the XOR output. The power consumed by the new latch can be reduced by gating its clock input, such gating has been proposed in [9] and it involves another XOR and OR gates, useful for high clock switching probability. It is subsequently shown that probability is very low and it is therefore not further being gated.

Figure 9 illustrates how LACG works. We call FF" target and FF' source. A target FF depends on K > 1 source FFs. It is required that the logic driving a target FF does not have an input externally of the block. Let X (D") denote the set of the XOR outputs of the source FFs, and denote by Q (D") the set of their corresponding outputs.

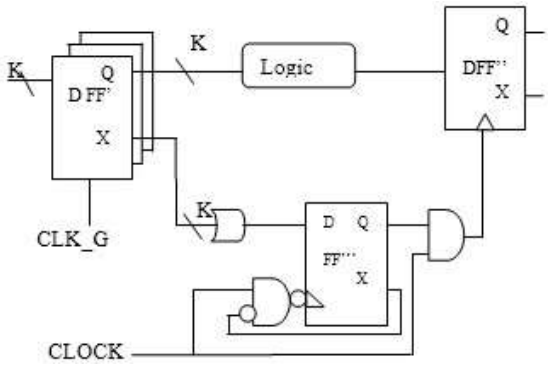

Fig. 9. LACG of general logic.

Let t and t+1 be two successive clock cycles shown in Figure.4.3, where the time tics refer to the rising edge of the clock pulses. We use the notation t -0.5 and t+0.5 to denote the clocks preceding and succeeding falling edges, respectively. Clearly ∑X(D")X(t)=0 is a sufficient condition for FF‟ not to change state at t+1 , where the summation means logical OR operation. FF‟s clock pulse could therefore be disabled at t+1 to save the switching power.

To generate the enabling signal obtained from data at t and ensure its validity at t+1, an oppositely clocked FF is introduced as shown in Figure. Upon the clocks falling edge at t + 0.5 there exists D'"(t+0.5)=∑X(D")X(t). Since FF'"is oppositely clocked, there exists Q'"(t+0.5)=D'"(t+0.5)=∑X(D")X(t). The signal Q'"is stable during the time period [t+0.5 ,t+1] obtaining Q'"(t+1)= ∑X(D")X(t).The gater Aext can then appropriately gate the clocks rising edge at t+1‟ which drives FF".Using a FF for gating is a considerable overhead that will consume power of its own. This can significantly be reduced by gating FF'"as shown in Figure 9.

Self-starting and Self-correcting counter implementation with look-Ahead clock gating (LACG) technique show in figure 10. LACG achieves 1). Better reduction in power dissipation by reducing the switching activity of clock signal. 2). Eliminates a very short time-window where the gating circuitry can properly work. 3). to reduce the hardware overhead involved and to maximize power savings. 4). Free from Serious timing constraints.

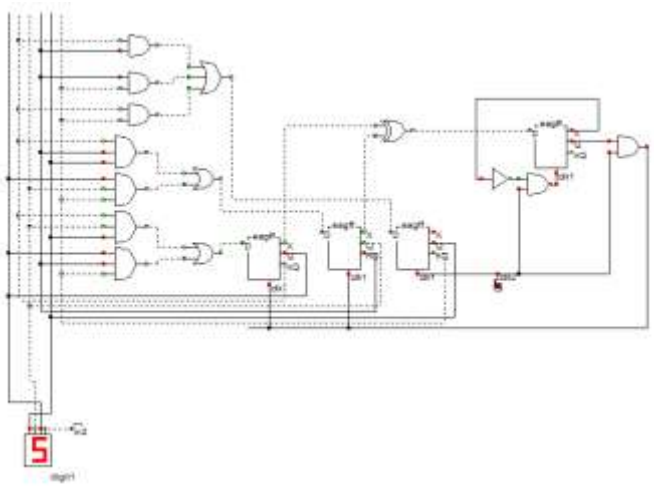

Fig.10.Self-Starting and Self-Correcting Counter with Look-Ahead clock gating (LACG).

To show LACG technique is best, the comparison is made between SSSC counter with data-driven clock gating and SSSC counter with LACG technique. The power values are also compared to the conventional SSSC counter. In data-driven clock gating there exist a serious timing problem for large applications but in LACG technique, the timing problem doesn't exist because of the full clock cycle allocation to determine the clock enable signal.

SIMULATION RESULTS

A novel Self-Starting and Self-Correcting Counter with Data-driven clock gating, Auto Gated Flip-Flops and Look – Ahead Clock Gating (LACG) is designed to reduce the dynamic power consumption. The simulation results and the power consumption values for the proposed technique are achieved using the simulation tool called Micro wind [10] . A Micro wind design system is Electronic Design Automation (EDA) software which produces software and hardware for Designing integrated circuits, System-On Chip (SOC) and printed circuit boards. The LACG technique is initially applied to single D flip-flop and the better power reduction is achieved. Then, the LACG technique is further applied to 4-bit, 8-bit, 16-bit and 32-bit Self-Starting and Self-Correcting Counter. The power consumption values for the various bits of SSSC counter are compared with the conventional SSSC counter and SSSC counter with the data-driven clock gating technique to show better power savings.

The simulation results for 3-bit, SSSC counter with conventional FFs, Data-driven clock gating method and LACG are shown in Fig.11, Fig12 and Fig15 respectively. The output wave forms for Auto Gated Flip-Flop and Enhanced AGFF with the XOR output are shown in fig13 and fig14 respectively.

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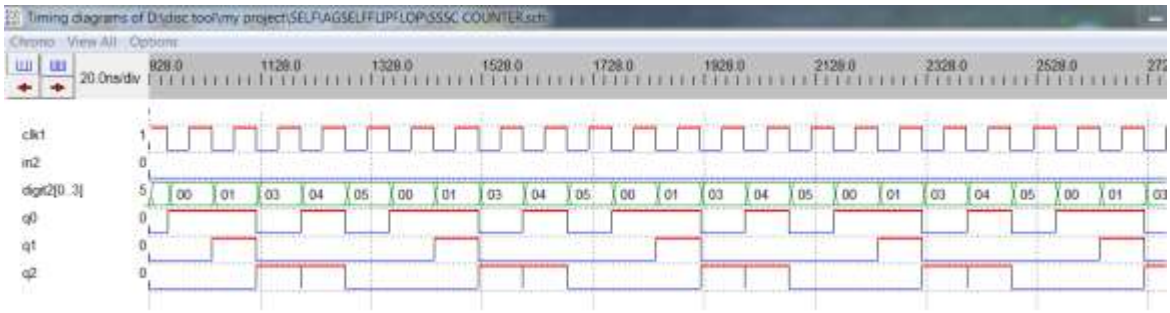

Fig.11. Output waveform for Self-Starting and Self-Correcting Counter circuit

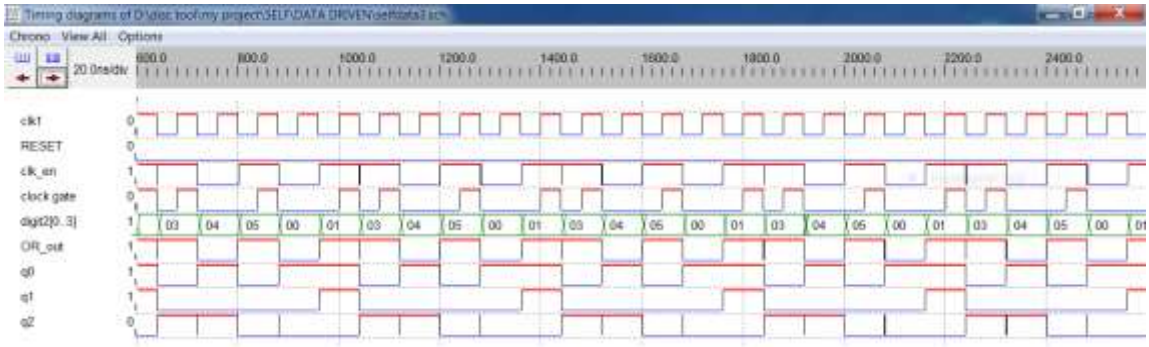

Fig: 12. Simulation result for 3-bit Self-Starting and Self-Correcting Counter with data-driven clock gating.

Fig.13. Output waveform for Auto Gated Flip-Flop.

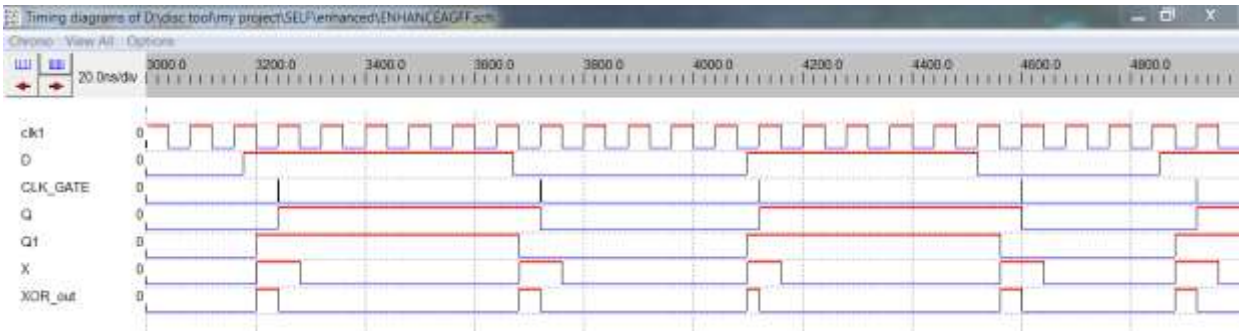

Fig.14.output waveform for enhanced AGFF with the XOR output

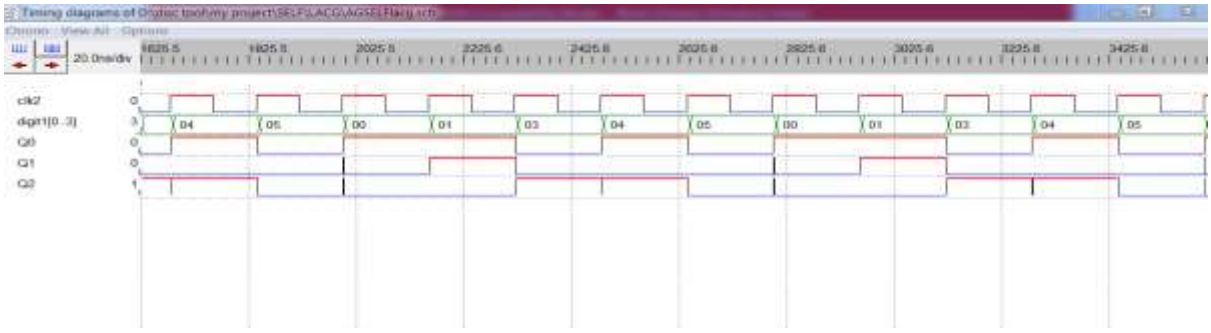

Fig.15. output wave form Self-Starting and Self-Correcting Counter with look-Ahead clock gating (LACG)

Table 1.Power dissipation comparison between Conventional FF and new design FFS.

Flip-Flops Names	Power dissipation(mw)
Conventional Flip-Flop	0.037
Auto Gated Flip-Flop	0.028
Enhanced AGFF	0.033

Power dissipation results: The Schematic diagram of Auto Gated Flip-Flop of Fig. 5 has been designed to transistor level for 0.8p-n technology. For all PMOS devices, W/L = 7.2p/0.8pm While For all NMOS devices, W/L = 3.6pm/0.8pn. The circuit was extracted from the layout, including parasitic, and simulated and Power dissipation results using Microwind & Dsch tools with a supply voltage of 5V. For comparison, a conventional flip-flop was also designed to transistor level with the same device sizing, and simulated. The Dsch tool simulation of Fig. 13 and Fig 14 shows correct circuit operation of AGFF and Enhanced AGFF. By using Microwind tool power dissipation comparison results shown in Table 1.

TABLE 2. POWER dissipation comparison between Conventional Flip-Flop, Data-driven clock gating technique and LACG.

SSSCcounter design techniques	***Power dissipation(mw)***
Conventional Flip-Flop	***0.066***
Data-driven clock gating technique	***0.069***
Look-Ahead clock gating (LACG)	***0.026***

From table II, it is observed that when compared to 3-bit conventional SSSCcounter and SSSCcounter with data-driven clock gating the proposed LACG technique reducing power dissipation of 65.43%. it is clear that the proposed SSSC counter with LACG achieves better power reduction compared to the conventional SSSCcounter and SSSCcounter with data-driven clock gating. The power dissipation of 3–bit SSSC counter is about 0.066mW

and the power consumption of 3 – bit SSSC counter with data-driven clock gating is about 0.069mW. Using LACG technique the power consumption has reduced to 0.026mW.

CONCLUSIONS

In this paper, we introduced a deterministic clock gating methodologies based on the observations of all the stages in a modern methods of reducing power dissipation. The simulation results clearly show that the proposed design has much less power dissipation compared to the ordinary Self-starting and Self-correcting counter without clock gating technique and to the data-driven clock gating technique. Results show that LACG is very effective in reducing clock power in high performance Self-starting and Self-correcting counter. We can also apply LACG technique to bigger applications like large number counting counters, Linear Feedback Shift Register, Built-In Self-Test (BIST) and cryptography.

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